In the Claims:

1-41. (Canceled)

42. (Currently Amended) Apparatus according to claim [[41]]57, wherein the host interface is adapted to receive the interrupt packet and to write the cause to a predetermined address in the memory, to be read by the CPU after the interrupt input is asserted.

43-44. (Canceled)

45. (Currently Amended) Apparatus according to claim [[44]]59, wherein the switched serial connection comprises a switch having a receive queue into which the serial interface places the data packets, and wherein the interrupt processor is adapted to place the interrupt packet into the receive queue following the data packets.

46-54. (Canceled)

55. (New) A method for communication between a peripheral device and a central processing unit (CPU), comprising:

receiving data from the peripheral device for transmission to a memory associated with the CPU;

receiving an interrupt signal from the peripheral device associated with the data;

sending one or more data packets containing the data over a switched serial connection to a host interface serving the memory and the CPU; and

sending an interrupt packet over the switched serial connection to the host interface, responsive to which an interrupt input of the CPU is asserted only after the one or more data packets have arrived at the host interface;

wherein receiving the data comprises receiving data to be written to the memory by direct memory access.

56. (New) A method for communication between a peripheral device and a central processing unit (CPU), comprising:

receiving data from the peripheral device for transmission to a memory associated with the CPU;

receiving an interrupt signal from the peripheral device associated with the data;

sending one or more data packets containing the data over a switched serial connection to a host interface serving the memory and the CPU; and

sending an interrupt packet over the switched serial connection to the host interface, responsive to which an interrupt input of the CPU is asserted only after the one or more data packets have arrived at the host interface;

wherein sending the one or more data packets comprises sending the data packets over a selected lane through a packet-switched network, and wherein sending the interrupt packet comprises sending the interrupt packet over the selected lane following the data packets.

57. (New) Communication apparatus, comprising:

a serial interface, which is operative to receive data from a peripheral device and to transmit the data in the form of one or more data packets via a switched serial

connection to a host interface, for writing to a memory associated with a central processing unit (CPU) served by the host interface; and

an interrupt processor, adapted to send an interrupt packet over the switched serial connection to the host interface to signal that the data have been transmitted, thus causing an interrupt input of the CPU to be asserted only after the one or more data packets have arrived at the host interface;

wherein the interrupt processor is operative to receive a cause of the interrupt from the peripheral device, and to incorporate the cause in the interrupt packet.

58. (New) Communication apparatus, comprising:

a serial interface, which is operative to receive data from a peripheral device and to transmit the data in the form of one or more data packets via a switched serial connection to a host interface, for writing to a memory associated with a central processing unit (CPU) served by the host interface; and

an interrupt processor, adapted to send an interrupt packet over the switched serial connection to the host interface to signal that the data have been transmitted, thus causing an interrupt input of the CPU to be asserted only after the one or more data packets have arrived at the host interface;

wherein the interrupt processor is adapted to send the interrupt packet after receiving an acknowledgment from the memory that the data have been written thereto.

59. (New) Communication apparatus, comprising:

a serial interface, which is operative to receive data from a peripheral device and to transmit the data in the form of one or more data packets via a switched serial

connection to a host interface, for writing to a memory associated with a central processing unit (CPU) served by the host interface; and

an interrupt processor, adapted to send an interrupt packet over the switched serial connection to the host interface to signal that the data have been transmitted, thus causing an interrupt input of the CPU to be asserted only after the one or more data packets have arrived at the host interface;

wherein the serial interface is coupled to send the data packets over a selected lane through the network, and wherein the processor is adapted to send the interrupt packet over the selected lane following the data packets.

60. (New) Communication apparatus, comprising:

a serial interface, which is operative to receive data from a peripheral device and to transmit the data in the form of one or more data packets via a switched serial connection to a host interface, for writing to a memory associated with a central processing unit (CPU) served by the host interface; and

an interrupt processor, adapted to send an interrupt packet over the switched serial connection to the host interface to signal that the data have been transmitted, thus causing an interrupt input of the CPU to be asserted only after the one or more data packets have arrived at the host interface;

wherein the switched serial connection is part of a switching fabric.

61. (New) Communication apparatus, comprising:

a host adapter, which is operative to receive data packets transmitted over a switched serial connection from a peripheral device, and to convey data from the packets for delivery to a memory associated with a CPU over a local bus that is

coupled to the memory and the CPU, and further to receive an interrupt packet sent over the switched serial connection responsive to an interrupt signal asserted by the peripheral device after sending the data to the memory; and

a host interface processor, adapted, responsive to the interrupt packet, to notify the CPU when all of the data have been conveyed to the local bus;

wherein the host adapter is operative to convey the data to the memory by direct memory access.

62. (New) Communication apparatus, comprising:

a host adapter, which is operative to receive data packets transmitted over a switched serial connection from a peripheral device, and to convey data from the packets for delivery to a memory associated with a CPU over a local bus that is coupled to the memory and the CPU, and further to receive an interrupt packet sent over the switched serial connection responsive to an interrupt signal asserted by the peripheral device after sending the data to the memory; and

a host interface processor, adapted, responsive to the interrupt packet, to notify the CPU when all of the data have been conveyed to the local bus;

wherein the switched serial connection is part of a switching fabric.